WHAT IS CLAIMED IS:

1. An antifuse device for an integrated circuit formed on a substrate, the antifuse device comprising:

a first layer of magnetic material formed on an exposed surface of the substrate;

a second layer of magnetic material positioned above the first layer;

a dielectric layer interposed between the first layer and the second layer wherein the first layer, the second layer and the dielectric layer form an MTJ junction; and

a logic circuit that is selectable so as to interconnect the first layer to a first electrical potential such that the first and second layers of magnetic material are shorted together when the logic circuit is selected.

2. The device of Claim 1, wherein the first layer comprises a pinned layer of magnetic material that is magnetized in a first fixed direction, the second layer comprises a soft layer of material that can be magnetized in either the first fixed direction or a second direction, and the dielectric layer comprises a tunnel dielectric layer interposed between the first layer and the second layer.

3. The device of Claim 2, wherein the first layer comprises a layer of NiFe that is approximately 100 -500Å thick, the second layer comprises a layer of NiFe that is approximately 40 - 50 Å thick, and the dielectric layer comprises a layer of Al_2O_3 that is approximately 10 – 15 Å thick.

4. The device of Claim 2, wherein the antifuse device has a resistance of greater than approximately 1 MegaOhm prior to the interconnection to the first electrical potential and wherein the antifuse device, upon interconnection to the first electrical potential is shorted across the tunnel dielectric layer.

5. The device of Claim 4, wherein the selected voltage is approximately 1.8 volts.

6. The device of Claim 1, wherein the antifuse MTJ device further comprises a first barrier layer, a pinning layer, and a second barrier layer.

7. The device of Claim 6, wherein the first barrier layer comprises a layer of Ta that is approximately 50 Å thick, the pinning layer comprises IrMn that is approximately 100 Å thick, and the second barrier layer comprises Ta that is approximately 200 Å thick.

8. A method of forming an MRAM device comprising:

simultaneously forming a plurality of first layers of magnetic material on a semiconductor substrate, wherein at least one of the first layers of magnetic material is for an antifuse device;

simultaneously forming a plurality of dielectric layers on the plurality of first layers of magnetic material wherein at least one of the dielectric layer is for the antifuse device;

simultaneously forming a plurality of second layers of magnetic material on a plurality of the dielectric layers wherein at least one of the second layers of magnetic material is for the antifuse device; and

electrically interconnecting the antifuse device to a source of electrical potential such that application of the electrical potential results in the antifuse device being shorted.

9. The method of Claim 8, wherein simultaneously forming a plurality of first layers of magnetic material comprises simultaneously forming a plurality of pinned layers of magnetic material that is magnetized in a first fixed direction.

10. The method of Claim 9, wherein simultaneously forming a plurality of pinned layers of magnetic material comprises forming a plurality of layers of NiFe that are approximately 100 -500Å thick.

11. The method of Claim 8, wherein simultaneously forming a plurality of dielectric layers comprises forming a plurality of tunnel dielectric layers on the plurality of first layers of magnetic material.

12. The method of Claim 11, wherein simultaneously forming a plurality of dielectric layers comprises simultaneously depositing a layer of Al_2O_3 having a

thickness of approximately 10 – 15 Å on the plurality of first layers of magnetic material.

13. The method of Claim 8, wherein simultaneously forming a plurality of second layers of magnetic material comprises forming a plurality of programmable second layers of magnetic material that can be magnetized by application of an external magnetic field in either the first fixed direction or in a second direction opposite the first fixed direction.

14. The method of Claim 13, wherein forming the plurality of programmable second layers comprises forming a plurality of layers of NiFe that are approximately 40 - 50 Å thick on the plurality of dielectric layers.

15. The method of Claim 8, wherein electrically interconnecting the antifuse device to a source of electrical potential comprises connecting the first magnetic layer to ground and applying an electrical potential to the second magnetic layer to an electrical potential of approximately 1.8 volts.

16. The method of Claim 15, wherein the application of the electrical potential to the second magnetic layer results in the resistance of the antifuse device changing from approximately 1 MegaOhms to 10 KiloOhms.